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S3	4	(graphics near hardware) and (differential adj equation\$1) and @ad<"20020401"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/02/11 18:42
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Volume 8, Issue 3, July-Sept. 2002 Page(s):223 - 238
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- ☐ **2. MIP-map level selection for texture mapping**
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- ☐ **3. Color recovery: true-color 8-bit interactive graphics**
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- ☐ **5. Controlled topology simplification**
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- ☐ **20. Efficient triangular surface approximations using wavelets and quadtree data structures**
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- ☐ **22. A reconfigurable multilevel parallel texture cache memory with 75-GB/s parallel cache replacement bandwidth**
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than when usage is priced. 20 References **Bohn**, R. Braun, H.W. Claffy, K. and Wolff, S.
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Visualization and Computer Graphics, IEEE Transactions on
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Newton, A.; Pederson, D.; Sangiovanni-Vincentelli, A.; Sequin, C.;
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- ☐ **4. A microprocessor with a 128-bit CPU, ten floating-point MAC's, four floating-point dividers, and an MPEG-2 decoder**
Suzuoki, M.; Kutaragi, K.; Hiroi, T.; Magoshi, H.; Okamoto, S.; Oka, M.; Ohba, A.; Yamamoto, Y.; Furuhashi, M.; Tanaka, M.; Yutaka, T.; Okada, T.; Nagamatsu, M.; Urakawa, Y.; Funyu, M.; Kunimatsu, A.; Goto, H.; Hashimoto, K.; Ide, N.; Murakami, H.; Ohtaguro, Y.; Aono, A.;
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- ☐ **2. SPAR: a new architecture for large finite element computations**
Taylor, V.E.; Ranade, A.; Messerschmitt, D.G.;
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Verde, C.;
[American Control Conference, 2001. Proceedings of the 2001](#)
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Marchal, P.; Sanchez, E.;
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- ☐ **10. Supercomputing-Japan: a competitive assessment**
Kahaner, D.K.; Wattenberg, U.;
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